REMARKS

In the IDS for the present application, a portion of the Wolf et al. ('Silicon Processing for the VLSI Era Volume 1: Process Technology') reference was cited. The Examiner has not acknowledged receipt of this reference. Applicants request that the Examiner acknowledge receipt of this reference.

Claims 1-2 and 8 stand "rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Specification [AAPA] in view of Wolf et al. ('Silicon Processing for the VLSI Era Volume 1: Process Technology', Lattice Press, 1986, pp. 182-194)." Claims 3-4, 6, and 10 stand "rejected under 35 U.S.C. § 103(a) as being unpatentable" over AAPA in view of Wolf, and further in view of Yoshizumi (U.S. Patent No. 5,444,012). Claims 5, 7, 9, and 28 stand "rejected under 35 U.S.C. § 103(a) as being unpatentable" over AAPA in view of Wolf, and further in view of Matsuura (U.S. Patent No. 5,132,774). Reconsideration and allowance of claims 1-10, and consideration and allowance of newly added claims 29-31, is respectfully requested.

Wolf provides an overview of silicon process technology in the VLSI (very large scale integration) field. Specifically, the Wolf reference provides a discussion of various properties of known films, for example, PECVD (plasma enhanced chemical-vapor deposition) film, APCVD (atmospheric pressure chemical-vapor deposition) film, and TEOS (tetraethyl orthosilicate) film.

Yoshizumi teaches a method of depositing a silicon oxide film that includes a first silicon depositing step on a bonding pad, a step of exposing the bonding pad by etching, and a second silicon depositing step (See Yoshizumi, Abstract). Therefore, a fuse element is covered by both the first and the second depositing steps, and the bonding pad is only covered by the second depositing step (Abstract). Yoshizumi does not teach an insulating film having a tensile stress.

Matsuura teaches a method of forming an interlayer insulating film that insulates first and second layers of conductor patterns in a semiconductor device (See Matsuura, Abstract). Matsuura does teach a TEOS APCVD film 14 that has tension stress; however, Matsuura teaches to relax the stress in metal conductor 12 by sandwiching film 14 between an upper and a lower insulating film

13 and 16 (See Matsuura, Column 6, line 64 through Column 7, line 6 and illustrated in Figure 5B). Therefore, the film 14 is not provided directly on the conductor 12, as the insulating film 13 is provided between them (Figure 5B). Because the films 13 and 16 are formed using silane gas and nitrous oxide, TEOS and O2, or as a PSG film using gas that has phosphine added to silane gas and O2, the films 13 and 16 have compressive stress (See Matsuura, Column 7, lines 3-15).

The Office Action provides that each feature of claim 1 is included in AAPA, except that AAPA "fails to disclose a second interlayer insulating film having a tensile stress." The Office Action further provides that "Wolf et. al. teach that it is well known in the art that a silicon oxide film formed by CVD process...would result in a film having a tensile stress..." Therefore, the Examiner has concluded that "it would have been obvious to one having skill in the art at the same time the invention was made to modify ... [AAPA] to include the limitation of a silicon oxide film formed by CVD."

Applicants respectfully traverse this conclusion.

Applicants' invention, as recited by claim 1, includes a feature that is neither disclosed nor suggested by the art of record, namely:

> A semiconductor device, comprising...a capacitor...a first interlayer insulating film...a first interconnect... [and] a second interlayer insulating film having a tensile stress provided so as to directly cover the first interconnect and the first interlayer insulating film...

This means that the semiconductor device recited in claim 1 includes a capacitor covered by a first interlayer insulating film. A first interconnect is provided on the first interlayer insulating film. A second interlayer insulating film having a tensile stress directly covers the first interconnect and the first interlayer insulating film.

Applicants' specification indicates that second interlayer insulating films have been used that have compressive stress (plasma TEOS films). At the time of Applicants' invention, there were no known problems with the use of a plasma TEOS second interlayer insulating film. Through research, Applicants

discovered that the plasma TEOS films used were producing components with undesirable characteristics.

For example, Applicants discovered that the plasma TEOS second interlayer insulating film prevented the polarization of the dielectric material forming the dielectric film 8 in the capacitor 10. This was a surprise, especially given the fact that the dielectric film 8 is separated from the plasma TEOS film by the upper electrode 9 and first interlayer insulating film 11 (See original specification, page 2, line 24 through page 3, line 29, and Figure 10D). Thus, the problems associated with plasma TEOS second interlayer insulating films were not known to one of ordinary skill in the art at the time that Applicants invention was made.

Additionally, Applicants discovered that these problems could be corrected by the use of a second interlayer insulating film having a tensile stress (e.g., ozone TEOS film). Although films having tensile stress were generally known (e.g., Wolf) at the time of Applicant's invention, the use of these films in semiconductor devices having capacitors as in claim 1 of the present application was not known. Because the problems associated with plasma TEOS films was not yet known at the time of Applicants' invention, it naturally follows that one skilled in the art would not know to correct these problems using films with tensile stress (ozone TEOS films).

Section 2143.01 of the MPEP provides that "[o]bviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art.". *See* MPEP § 2143.01, *citing* In re Kotzab, 217 F.3d 1365,1370, (Fed. Cir. 2000); In re Fine, 837 F.2d 1071 (Fed. Cir. 1988); and In re Jones, 958 F.2d 347 (Fed. Cir. 1992).

For the present application, there was no teaching, suggestion, or motivation to combine AAPA with Wolf. This is clear because Applicants discovered the cited problems with the use of the plasma TEOS films (having compressive and not tensile stress), which was an unexpected problem. Further, although Wolf discusses films generally (including films with tensile stress), Wolf provides no indication that a film with tensile stress could be used to alleviate poor

dielectric film characteristics in a capacitor. In fact, Wolf does not disclose using a film with tensile stress in a capacitor application whatsoever.

Thus, Applicants respectfully traverse the rejection of claim 1 under 35 U.S.C. § 103(a) over the combination of AAPA and Wolf. Neither Yoshizumi, Matsuura, nor any of the other references of record make up for the above-described deficiencies of AAPA and Wolf. Therefore, claim 1 is patentable over the art of record.

Claims 2-10, and newly added claims 29-31, include all of the features of independent claim 1 from which they depend. Accordingly, claims 2-10, and 29-31 are also patentable over the art of record.

Newly added claim 29 recites a second interlayer insulating film that "provides substantially flat step coverage of the first interconnect and the first interlayer insulating film." This amendment is clearly supported in the originally filed specification at, for example, page 10, lines 9-20, page 19, lines 3-10, and page 32, lines 1-7.

This means that when the second interlayer insulating film is being formed, the film performs self-reflow and results in a film with no step, that is, a film that is substantially flat. This is in contrast to conformal step coverage, in which the film is uniform in thickness. In conformal step coverage, a thicker film layer is required, which results in additional stress to the capacitor (See Specification, page 10, lines 12-24).

AAPA does not disclose a second interlayer insulating film that provides substantially flat step coverage on the first film and first interconnect. Neither Wolf, Yoshizumi, nor Matsuura, make up for the deficiencies of AAPA with respect to claim 29 of the present application.

Wolf does disclose films which provide good step coverage; however, these films are limited to those formed using a PECVD method (See Table 2 on page 183, and pages 186-187 generally). Further, Wolf teaches to form TEOS films by LPCVD, not PECVD. In fact, Wolf explicitly provides that TEOS films provide conformal step coverage (See Table 2 on page 183, and page 184 generally). Wolf defines conformal step coverage as "coverage in which equal

film thickness exists over all substrate topography regardless of its slope" (See Figure 17a, and first paragraph of the section entitled "Step Coverage of As-Deposited CVD SiO_2 Films" on page 185). Conformal coverage is not "substantially flat step coverage" as defined in amended claim 1, because "substantially flat step coverage" is where the top surface of the overlaying film is planar; that is, has no step (See original specification, page 10, lines 12-17).

Thus, Wolf does not teach or suggest forming a second interlayer insulating film that provides substantially flat step coverage on the first interconnect and first interlayer insulating film.

Therefore, claim 29 is patentable over the art of record for this additional reason.

Newly added claim 30 includes the limitation of a dielectric film including a remnant polarization of approximately 10 $\mu C/cm^2$, and newly added claim 31 includes the limitation of a dielectric film including a remnant polarization of at least 10 $\mu C/cm^2$. These features are supported by the original application at page 23, lines 19-25, and further at page 25, lines 28-32. No new matter has been added.

None of the cited references disclose the features specified in claims 30-31. Further, prior to Applicant's invention, plasma TEOS films were used as second interlayer insulating films. Because plasma TEOS second interlayer insulating films have compressive stress, the dielectric films in the capacitor exhibit less desirable characteristics. For example, Applicants research and testing indicates that the dielectric film in a prior art capacitor (e.g., in a device with a plasma TEOS second interlayer insulating film) has a remnant polarization of 3 $\mu C/cm^2$ (See original specification, page 23, lines 16-19).

Accordingly, newly added claims 30-31 are patentable over the art of record irrespective of their dependence on claim 1.

In view of the amendments and arguments set forth above, the above-identified application is in condition for allowance which action is respectfully requested.

Request for Extension of Time:

In the subject application, it is requested that the shortened period for responding to the Official Action dated August 10, 2001 be extended two months until January 10, 2002. Enclosed is the Patent Application processing fee under 37 C.F.R. § 1.17.

Respectfully Submitted,

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Enclosures:
Version with markings to show changes made
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The Assistant Commissioner for Patents is hereby authorized to charge payment to Deposit Account No. **18-0350** of any fees associated with this communication.

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I hereby certify that this paper and fee are being deposited, under 37 C.F.R. § 1.10 and with sufficient postage, using the "Express Mail Post Office to Addressee" service of the United States Postal Service on the date indicated above and that the deposit is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Kathleen Libby

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

CLAIMS:

Claim 28 is cancelled.

Claims 29-31 have been newly added.